DSP Algorithm based Enhanced Phase Locked Loop Scheme for DSTATCOM

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Abstract–This paper deals with Enhanced Phase Locked Loop Control scheme for Distributed Static Compensator (DSTATCOM) in the distribution system. The proposed control scheme based DSTATCOM eliminates current harmonics, maintains unity power factor at source, zero voltage regulation and load balancing. The Enhanced Phase Locked Loop (EPLL) Control scheme is based on Digital Signal Processing (DSP) which is used to extract fundamental component of active and reactive currents for generation of reference source currents. The DSTATCOM consists of six-leg based voltage source converter (VSC) which uses uni-polar switching which doubles the switching frequency and reduces size of the filtering circuit. The zig-zag/three single-phase transformers reduce DC bus voltage and acts as a neutral current compensator. The proposed control scheme for six-leg DSTATCOM is modeled and validated in MATLAB R2012b by using simpower systems toolbox.

Keywords–Distributed static compensator (DSTATCOM), unity power factor, zero voltage regulation, enhanced phase locked loop (EPLL), distribution system, resonant converter, simulation, ac analysis.

I. INTRODUCTION

Three phase four wire systems have been used to supply single-phase linear/non-linear loads, such as office automation machines, fans, computer loads, lighting ballasts etc in the distribution systems. These loads in the distribution system experience severe power quality (PQ) problems, such as high reactive power requirement, poor voltage regulation, current harmonics, excessive neutral current, voltage flicker, sag, swell and load unbalancing [1–3]. To limit PQ problems, IEEE and IEC have proposed many standards such as IEEE Std.141-1993, IEEE Std. 519-1992, IEC 1000-3-2 etc. [4–6]. Custom Power Devices (CPDs) are used as solutions for problems discussed in the literature. DSTATCOM is proposed for mitigation of PQ problems in the current, Dynamic Voltage Restorer (DVR) is used for compensating the PQ problems in the voltage whereas the Unified Power-Quality Conditioner (UPQC) is proposed for compensating both current and voltage problems. The DSTATCOM is a shunt connected CPD used for power factor correction, zero voltage regulation, current harmonic suppression and load balancing. The review of control algorithms and its development are discussed in many papers [7–9]. The performance of DSTATCOM mainly depends upon quick extraction of reference currents using control algorithms [10]. Different Phase Locked Loop (PLL) techniques are described for accurate and reliable control [11]. The various classifications of phased locked loops are Parke PLL, adaptive SRF-PLL, multi-complex coefficient-filter based PLL, EPLL, and Power based PLL for various applications [12-16].

In this paper, DSP Algorithm based Enhanced Phase Locked Loop Control Scheme for DSTATCOM is proposed to eliminate the current harmonics, corrects the Power factor, regulates the terminal voltage and balances the source current even when the load currents are unbalanced. The features of DSP based EPLL scheme is

i. Control scheme is simple and hardware implementation in DSP is easy.
ii. EPLL scheme adopts deviations in amplitude of the voltage, phase angle and frequency of input and gives fast accurate response.
iii. It will extract accurate fundamental components from distribution system or supply [17-20].

Three phase four-wire neutral current consists of triplen harmonic currents and zero-sequence neutral currents passing through neutral conductor and hence overloads it. An isolated zig-zag/three single phase transformer is used to mitigate excessive neutral currents [21–23].

II. DSTATCOM SYSTEM CONFIGURATION

The schematic diagram of six-leg VSC based DSTATCOM with EPLL control algorithm is shown in Fig.1. The proposed DSTATCOM is connected at Point of Common Coupling (PCC) of three phase supply having source impedance and three phase linear/non-linear load. The DSTATCOM consists of twelve IGBTs based voltage source converter (VSC) through three interfacing inductors on the ac side and one capacitor on dc side. A six-leg IGBT VSC based requires uni-polar switching and doubles switching frequency so that higher order harmonics can be eliminated by using filter circuit. The DSTATCOM injects compensating currents (i_{ca}, i_{cb}, i_{cc}) in such a way that elimination harmonics, unity power factor at the source, zero voltage regulation and load balancing. A Ripple filter consists of resistance (R_f) and capacitance (C_f) connected across PCC to compensate high frequency voltage harmonics.

The transformer primary winding is connected in zigzag connection and secondary winding is connected to three single phase transformer so as to reduce DC bus voltage. The isolated zigzag/three single phase transformer is used to compensate neutral current. The zigzag transformer is designed in such a way that magneto motive force (mmf) is balanced in all three phases of the transformer. The design and selection of DSTATCOM and zigzag/three single phase transformers is explained in the following section.

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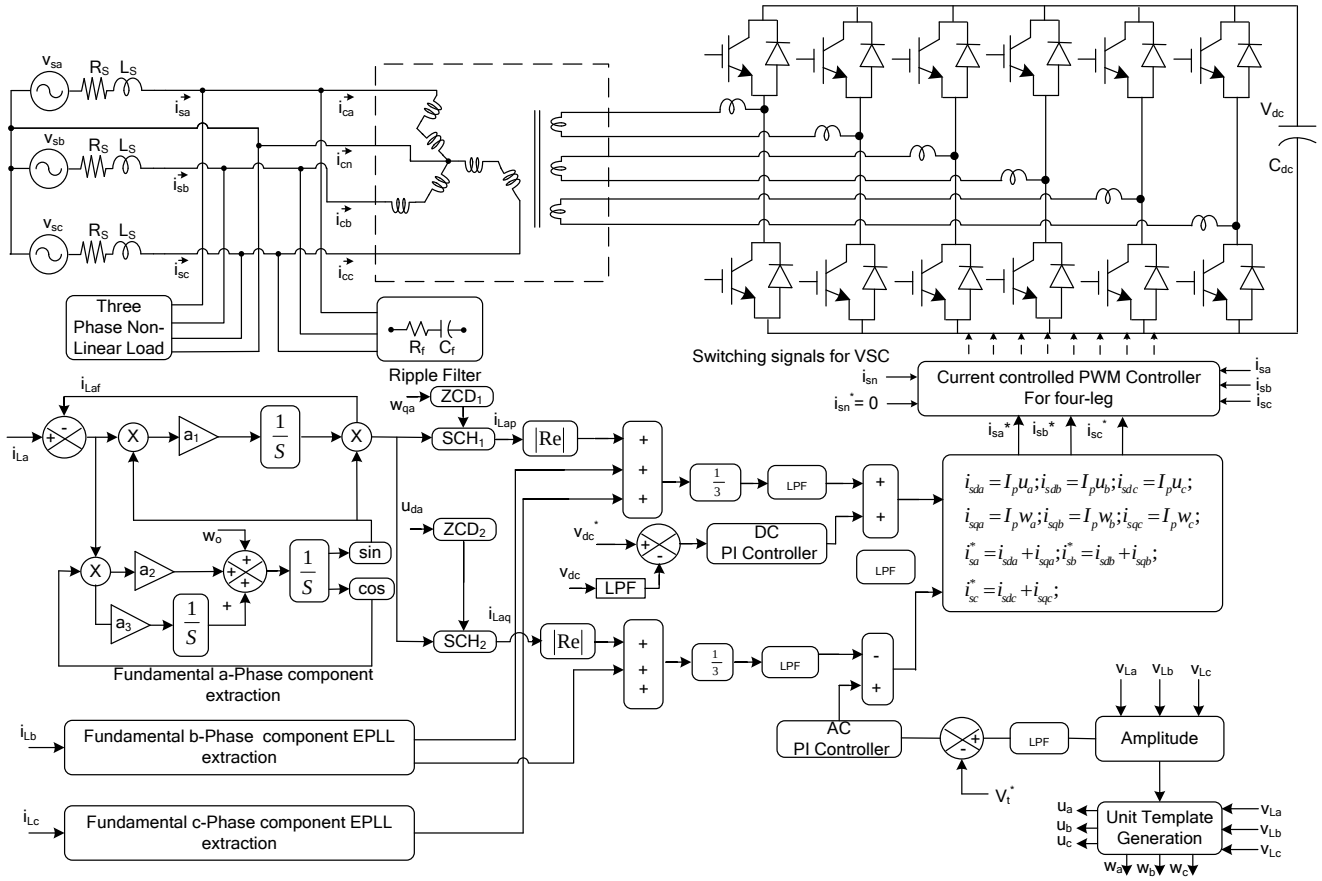

Fig.1 Schematic diagram and control algorithm of six-leg VSC based DSTATCOM

A. Design and selection of zigzag transformer

V_{a1}, V_{a2}, V_{b1}, V_{b2}, V_{c1}, V_{c2} are the voltages across each phase winding and V_a, V_b, V_c are resultant voltages of each phase winding which are shown in Fig. 2.

Assume that input voltage to zig-zag transformer (V_{ab}) =415V then per phase voltage of each winding are $V_{an}=V_{bn}=V_{cn}$=239.6V, $V_{a1}=V_{b1}=V_{c1}$=138.33V and $V_{a2}= V_{b2}= V_{c2}$=138.33V.

B. Design and selection of DSTATCOM

Table.1 shows design and selection values of six-leg DSTATCOM. It consists of DC bus capacitor, DC bus capacitor voltage, ripple filter (R_f and C_f) and Interface inductor(L_{ac}).where V_L is voltage of three phase transformer which is taken as 239.6 V, modulation index (m) is 1, minimum voltage level (V_{mindc}) is 391.26 V, DC bus reference voltage (V_{dc}) is selected as 400V by using zig-zag/three single phase transformer, overloading factor (k) is taken as 1.1, phase current (I_{ph}) is taken as 25 A, phase voltage (V_{ph}) is taken as 239.60 V, time (t) is taken as 250 µs, peak-peak value of current ripple (i_{cp-p}) is taken as 5%, PWM switching frequency (f_s) is taken as 20 kHz , interface ac inductance (L_f) is taken as 2.0 mH, ripple filter series resistance (R_f) is taken as 5 Ω and ripple filter series capacitance (C_f) is taken as 6 µF.

III. PROPOSED CONTROL SCHEME

The dynamic performance of a DSTATCOM is based upon quick and accurate extraction of fundamental component of load currents. Fig.1. shows schematic diagram and Enhanced Phase Locked Loop control Scheme for DSTATCOM to estimate reference source currents. The three-phase supply voltage/phase are v_{sa}, v_{sb}, v_{sc}, three phase supply currents are i_{sa}, i_{sb}, i_{sc}, three phase compensating currents are i_{ca}, i_{cb}, i_{cc}, three phase reference source currents are i_{sa}^*, i_{sb}^*, i_{sc}^*,three phase load currents are i_{La}, i_{Lb}, i_{Lc} and reference DC bus voltage is v_{dc}.

The three phase supply voltages/phase (v_{sa},v_{sb},v_{sc}) can be represented as follows:

$$v_{sa} = v_{mp}\cos(\omega t) \quad (1)$$

$$v_{sb} = v_{mp}\cos(\omega t - 120^\circ) \quad (2)$$

$$v_{sc} = v_{mp}\cos(\omega t - 240^\circ) \quad (3)$$

where v_{mp} is the maximum value of phase supply voltage.

The resultant magnitude of three phase supply voltages can be determined as

$$v_t = \left[2/3\left(v_{sa}^2 + v_{sb}^2 + v_{sc}^2\right)\right]^{1/2} \quad (4)$$

The three supply voltages v_{sa}, v_{sb} and v_{sc} corresponding to in-phase components of unit templates are

$$u_{da} = v_{sa}/v_t, u_{db} = v_{sb}/v_t, u_{dc} = v_{sc}/v_t \quad (5)$$

The three supply voltages v_{sa}, v_{sb} and v_{sc} corresponding to quadrature-phase components of unit templates are

$$w_{qa} = -u_{db}/\sqrt{3} + u_{dc}/\sqrt{3} \quad (6)$$

$$w_{qb} = \sqrt{3}u_{da}/2 + (u_{db} - u_{dc})/2\sqrt{3} \quad (7)$$

$$w_{qc} = -\sqrt{3}u_{da}/2 + (u_{db} - u_{dc})/2\sqrt{3} \quad (8)$$

Table 1: Design and selection of DSTATCOM parameters

Design Parameter	Formulae	Calculated value	Selected value
DC bus Capacitor Voltage	$V_{dc} = 2\sqrt{2}V_L / \sqrt{3}m$	V_{dc}= 391.2652V	V_{dc}=400V
DC Bus Capacitor	$\frac{1}{2}C_{dc}[(V_{dc}^2)-(V_{dc\,mn}^2)] = 3V_{ph}(kI_{ph})t$	C_{dc} = 2600μF	C_{dc} = 3000μF
Interface AC Inductor	$L_{ac} = (\sqrt{3}mV_{dc})/(12kf_s i_{cp-p})$	L_f=1.9mH	L_f=2.0 mH
Ripple filter	$Z_f = \sqrt{(R_f^2 + X_c^2}$, $X_f = \frac{1}{2\pi f_s L_f}$	Z_f=637Ω	Z_f=637 Ω

The load harmonic currents can be represented by

$$i_{La} = \sum_{k=1}^{\infty} i_{kLa} \cos(k\omega t - \varphi_{ak}) \quad (9)$$

$$i_{Lb} = \sum_{k=1}^{\infty} i_{kLb} \cos(k\omega t - \varphi_{bk} - \frac{2\pi}{3}) \quad (10)$$

$$i_{Lc} = \sum_{k=1}^{\infty} i_{kLc} \cos(k\omega t - \varphi_{ck} + \frac{2\pi}{3}) \quad (11)$$

where i_{kLa}, i_{kLb}, i_{kLc} are the amplitudes of k^{th} harmonic load currents. The Φ_{ak}, Φ_{bk}, Φ_{ck} are the phase angles between supply voltage and k^{th} harmonic load currents.

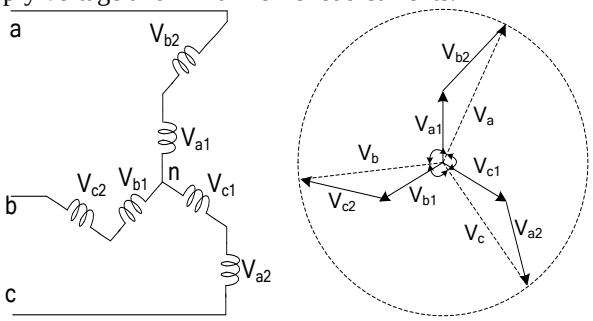

Fig. 2: Zig-zag transformer and phasor diagram

The fundamental load component of each phase current can be estimated by using proposed DSP Algorithm based EPLL control scheme. In this proposed control scheme each phase 'a' extracts input signal from the load current (i_{La}).The error signal (i_{err}) is obtained by the difference between load current (i_{La}) and fundamental load current (i_{Laf}). In this DSP Algorithm based EPLL control scheme internal parameters a_1, a_2 and a_3 are selected as (15), (9) and (1) respectively used to control transient and steady state [17-18]. Similarly other two phase fundamental load currents (i_{Lbf} and i_{Lcf}) are also extracted in the same manner. The phase 'a' fundamental component of load current (i_{Laf}) is in phase with input current signal (i_{La}) and it has phase shift with reference to in-phase unit templates (w_{qa}).

To extract amplitude of reactive power component of fundamental load current, Zero Crossing Detector (ZCD_2) is used on in-phase quadrature templates (u_{da}) are used. The extracted fundamental load current (I_{Laf}) is taken as input to Sample and Hold Circuit (SHC_2) and Zero Crossing Detector (ZCD_2) is used for trigger pulses block. The output of SHC_2 is considered as amplitude of fundamental reactive component load current (I_{Laq}). Similarly other two phase reactive power components of fundamental load current (I_{Lbq} and I_{Lcq}) are also estimated. The average active and reactive power component of fundamental load current is calculated as

$$I_{Lp} = (I_{Lap} + I_{Lbp} + I_{Lcp})/3 \quad (12)$$

$$I_{Lq} = (I_{Laq} + I_{Lbq} + I_{Lcq})/3 \quad (13)$$

These DC component currents are passed through Low Pass Filter (LPF) to extract the active and reactive currents I_{Lp} and I_{Lq}.

i. Unity power factor (UPF) operation of DSTATCOM

The difference between reference DC bus capacitor voltage and actual DC bus voltage of DSTATCOM is taken as error in the DC bus. This error is given to Proportional Integral (PI) controller and output of PI is considered as current loss component (I_{lsp}) and is added to active component of current (i_{Lp}).

$$I_{lsp(m)} = I_{lsp(m-1)} + K_{dp}(V_{dc(m)} - V_{dc(m-1)}) + K_{di}V_{dc(m)} \quad (14)$$

where the error in DC bus at m^{th} sample instant is given by $V_{dc(m)}=V_{dc}^{*}-V_{dc(m)}$. The K_{dp} and K_{di} are proportional and integral constants of PI controller.

The reference active component of source current is calculated as

$$I_p = I_{Lp} + I_{lsp} \quad (15)$$

ii. Zero voltage Regulation operation of DSTATCOM

The source current delivers same active component current I_p along with reactive power component I_q. The difference between actual amplitude of terminal voltage at PCC (V_t) and reference terminal voltage is taken as error at the AC bus.

$$I_{lsp(m)} = I_{lsp(m-1)} + K_{qp}(V_{t(m)} - V_{t(m-1)}) + K_{qi}V_{t(m)} \quad (16)$$

where the error in AC bus at m^{th} sample instant is given by $Vt_{(m)}=V_t^{*}-V_{t(m)}$. The K_{qp} and K_{qi} are proportional and integral constants of PI controller. This error is given to Proportional Integral (PI) controller and output of PI is considered as current loss component (I_{lsq}) and added to active component current (I_{Lq}).

$$I_q = I_{Lq} - I_{lsq} \quad (17)$$

iii. Reference source currents estimation and generation of gating pulses

The three phase reference active and reference source currents can be generated by using in-phase unit templates,

quadrature unit templates, active power component and reactive power components.

$$i_{sda} = I_p u_{da}, i_{sdb} = I_p u_{db}, i_{sdc} = I_p u_{dc} \quad (18)$$

$$i_{sqa} = I_q u_{qa}, i_{sqb} = I_q u_{qb}, i_{sqc} = I_q u_{qc} \quad (19)$$

The three phase reference source currents (i_{sa}^*,i_{sb}^*,i_{sc}^*) can be generated by

$$i_{sa}^* = i_{sda} + i_{sqa} \quad (20)$$

$$i_{sb}^* = i_{sdb} + i_{sqb} \quad (21)$$

$$i_{sc}^* = i_{sdc} + i_{sqc} \quad (22)$$

iv. Current Controlled PWM Generator for six-leg VSC

The error currents are obtained by the difference between reference source currents (i_{sa}^* , i_{sb}^* , i_{sc}^*) and source currents (i_{sa} , i_{sb} , i_{sc}). The equations are given by

$$i_{aer} = i_{sa}^* - i_{sa} \quad (23)$$

$$i_{ber} = i_{sb}^* - i_{sb} \quad (24)$$

$$i_{cer} = i_{sc}^* - i_{sc} \quad (25)$$

To generate uni-polar gating pulses for six-leg VSC, the error-current signals (i_{aer},i_{ber}, i_{cer}) are compared with triangular wave (i_{tri}). The uni-polar switching doubles the PWM switching frequency so that it reduces the filter circuit requirement and improves performance of DSTATCOM.

$i_{aer} > i_{tri}$ (phase 'a' in the left-leg VSC upper switch is on)
$i_{aer} \leq i_{tri}$ (phase 'a' in the left-leg VSC lower switch is on)
$-i_{aer} > i_{tri}$ (phase 'a' in the right-leg VSC upper switch is on)
$-i_{aer} \leq i_{tri}$ (phase 'a' in the right-leg VSC lower switch is on)
Similar logic is used for other two phases of H-bridge VSC.

v. Computation of PI Controller Gains

The DC and AC PI controller gains constants obtained using the Ziegler–Nichols step response technique. A step input of amplitude (U) is applied and the output response of the dc bus voltage is obtained for the open-loop system. The maximum gradient (G) and the point at which the line of maximum gradient crosses the time axis (T) are computed. The gains of the controller are computed using the following equations:

$$K_p = \left|1.2U / GT\right| \quad (26)$$

$$K_p = \left|0.6U / GT^2\right| \quad (27)$$

The gain values for both the DC and AC PI controllers are computed and are given in the Appendix.

IV. Simulation Results and Discussion

DSP Algorithm based EPLL control scheme based DSTATCOM along with zig-zag/three single phase transformer is modeled using MATLAB and simulation results are demonstrated for unity power factor, zero voltage regulation, elimination of harmonics, neutral current compensation and load balancing for three linear/non-linear loads.

A. Performance of EPLL control scheme based DSTATCOM with linear loads for neutral current compensation and UPF operation

The dynamic performance of EPLL control scheme based DSTATCOM with linear loads balanced/unbalanced condition under UPF operation is depicted in Fig. 3. At t=0.75 sec, three phase load is changed to two phase load and at t= 0.85 sec again two phase load is changed to three phase load. The three phase supply voltages (v_{sa} ,v_{sb} ,v_{sc}), source currents (i_{sa},i_{sb},i_{sc}), load currents (i_{La},i_{Lb},i_{Lc}), compensating currents (i_{ca},i_{cb},i_{cc}), source neutral current (i_{sn}), load neutral current (i_{Ln}), DC bus voltage (v_{dc}) and terminal voltage(v_t) are depicted in Fig.3. At different variations in three phase load, it is observed that supply voltages, source currents are balanced and harmonic free, supply neutral current is almost zero, DC bus voltage is maintained close to reference DC bus voltage of 400V and unity power factor at the source voltage and source current .

B. Performance of EPLL control scheme based DSTATCOM with non-linear loads for neutral current compensation and UPF operation

The dynamic performance of EPLL control scheme based DSTATCOM with Non-linear loads balanced/unbalanced condition under UPF operation is depicted in Fig. 4. At t=0.75 sec, three phase load is changed to two phase load and at t= 0.85 sec again two phase load is changed to three phase load. The three phase supply voltages (v_{sa}, v_{sb}, v_{sc}), source currents (i_{sa}, i_{sb}, i_{sc}), load currents (i_{La}, i_{Lb}, i_{Lc}), compensating current (i_{ca},i_{cb},i_{cc}),source neutral current (i_{sn}), load neutral current(i_{Ln}),DC bus voltage(v_{dc}) and terminal voltage(v_t) are depicted in Fig .4. At different variations in three phase load it was observed that supply voltages, source currents are balanced and harmonic free, supply neutral current is almost zero, DC bus voltage is maintained close to reference DC bus voltage of 400V and unity power factor at the source voltage and source current. The source voltage and source current THDs are 2.59% and 2.78% whereas load THD is 91.55%.

C. Performance of EPLL control scheme based DSTATCOM with linear loads for neutral current compensation and zero voltage regulation operation

The dynamic performance of EPLL control scheme based DSTATCOM with linear loads balanced/unbalanced condition under zero voltage regulation operation is depicted in Fig. 5. At t=0.75 sec, three phase load is changed to two phase load and at t= 0.85 sec again two phase load is changed to three phase load. The three phase supply voltages (v_{sa},v_{sb},v_{sc}), source currents(i_{sa},i_{sb},i_{sc}), load currents (i_{La},i_{Lb},i_{Lc}), compensating current (i_{ca},i_{cb},i_{cc}) source neutral current (i_{sn}), load neutral current (i_{Ln}), DC bus voltage (v_{dc}) and terminal voltage (v_t) are depicted in Fig .5. At different variations in three phase load it is observed that supply voltages, source currents are balanced and harmonic free, supply neutral current is almost zero, unity power factor at the source, DC bus voltage and voltage at PCC are maintained close to reference values of 400V and 339 V respectively.

D. Performance of EPLL control scheme based DSTATCOM with Non-linear loads for neutral current compensation and zero voltage regulation operation

The dynamic performance of EPLL control scheme based

DSTATCOM with non-linear loads balanced/unbalanced condition under zero voltage regulation operation is depicted in Fig. 6. At t=0.75 sec, three phase load is changed to two phase load and at t= 0.85sec again two phase load load is changed to three phase load. The three phase supply voltages (v_{sa}, v_{sb}, v_{sc}), source currents (i_{sa}, i_{sb}).

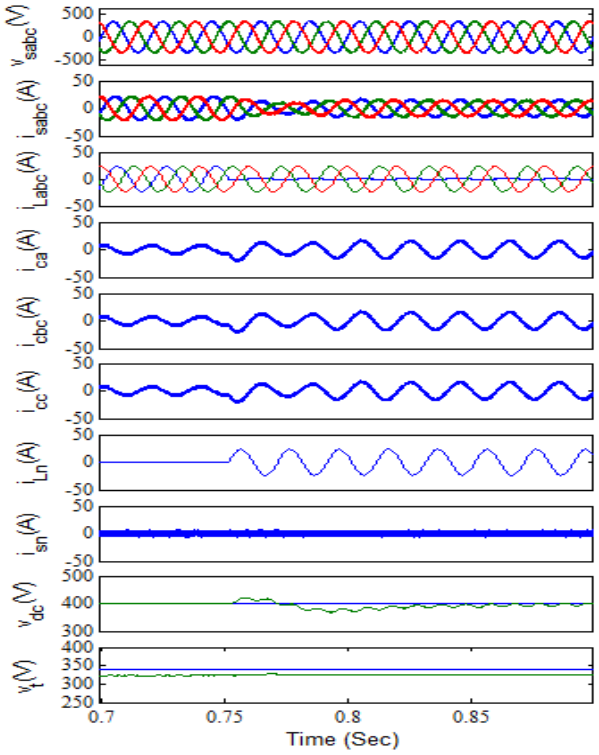

Fig. 3: Performance of DSP algorithm based EPLL control scheme for DSTATCOM with linear loads under UPF operation.

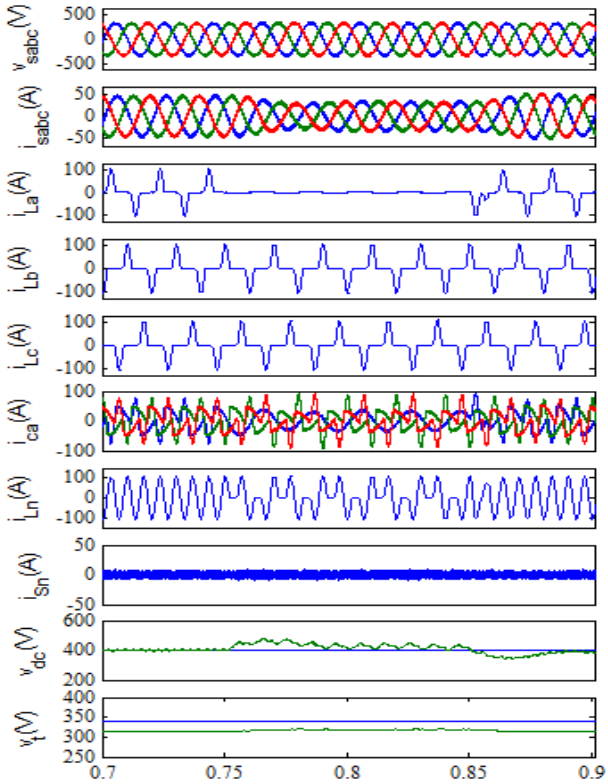

Fig. 4: Performance of DSP algorithm based EPLL control scheme for DSTATCOM with non-linear loads under UPF operation.

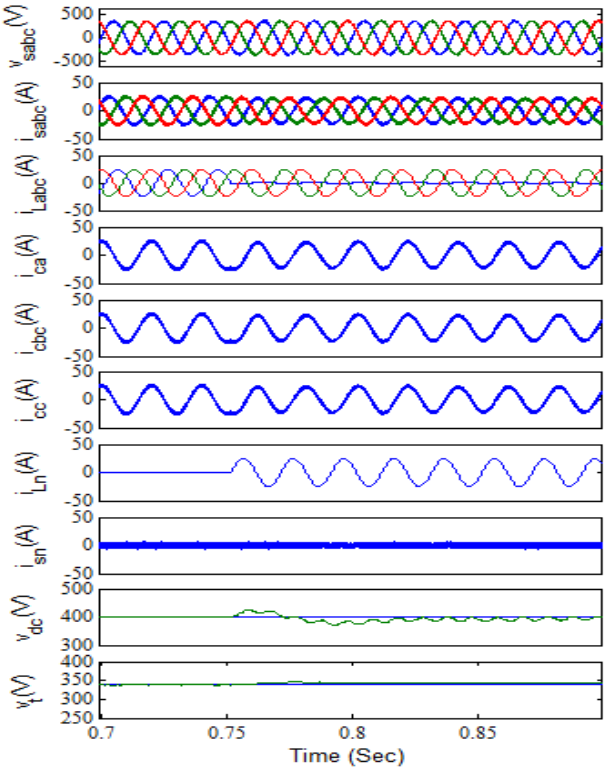

Fig. 5: Performance of DSP algorithm based EPLL Control scheme for DSTATCOM with linear loads under zero voltage regulation operation.

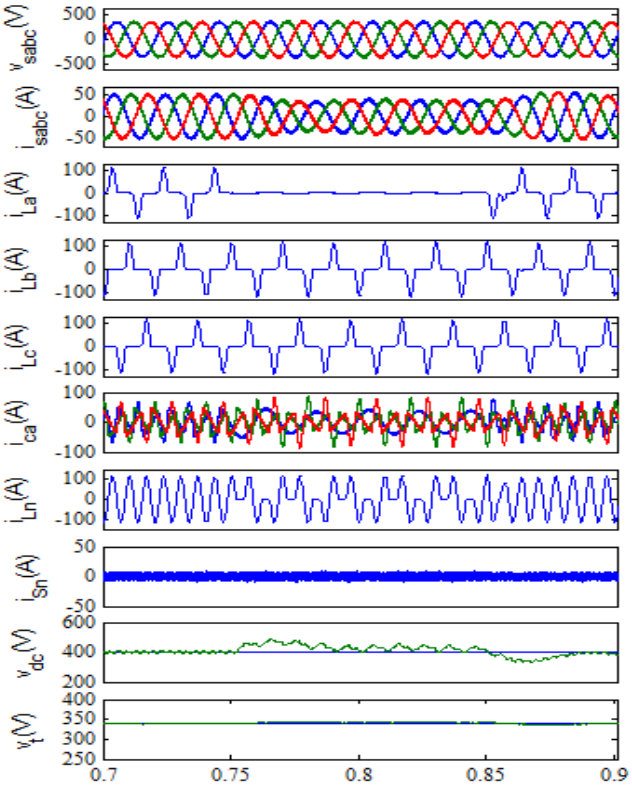

Fig. 6: Performance of DSP Algorithm based EPLL Control scheme for DSTATCOM with non-linear loads under zero voltage regulation operation

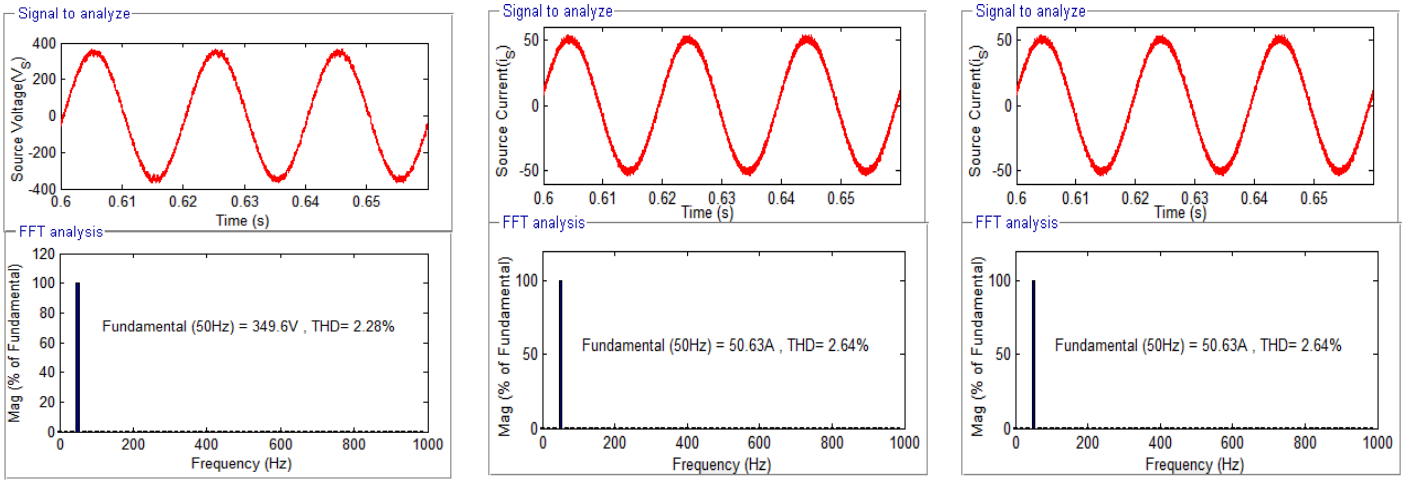

Fig. 7: Harmonic spectra of source voltage, source current and load current.

i_{sc}),load currents (i_{La}, i_{Lb}, i_{Lc}), compensating current(i_{ca}, i_{cb}, i_{cc}), source neutral current (i_{sn}), load neutral current (i_{Ln}), DC bus voltage (v_{dc}) and terminal voltage (v_t) are depicted in Fig .6. At different variations in three phase load it was observed that supply voltages, source currents are balanced and harmonic free, supply neutral current is almost zero, unity power factor at the source, DC bus voltage and voltage at PCC are maintained close to reference values of 400V and 339V respectively. The source voltage and source current THD are 2.28% and 2.64% whereas load THD is 91.85% are shown in Fig.7.

VI. Conclusion

The dynamic performance of DSP Algorithm based EPLL control scheme for six-leg VSC based DSTATCOM with linear/non-linear loads gives satisfactory results. The performance of DSTATCOM demonstrated for neutral current compensation under unity power factor and zero voltage regulation modes along with harmonic elimination. The zigzag/three single phase transformers has maintained source neutral current which is almost equal to zero and act as a neutral current compensator. The six-leg VSC uses uni-polar switching which doubles frequency so that filter requirement is reduced. The DC bus voltage is regulated to reference value of 400V in all variations of loads during unity power factor and zero voltage regulation operation. The terminal voltage is regulated to reference value of 339V in all variations of load during zero voltage regulation. The three phase non-linear load draws a load current of total harmonic distortion (THD) of 91.85% whereas source voltage and current are having a THD of 2.28% and 2.64% respectively. These THDs of source voltage and source currents are within the limits of IEEE-519 & IEC 1000-3-2 standards.

Appendix

Three phase supply line voltage: 415V, 50Hz
Supply Impedance: R_s=0.04Ω, L_s=4mH
Loads:
i. *Linear load*: R_L=12 Ω and L=25mH
ii.*Non-linear loads*: *Three single phase diode bridge rectifier with R*=12 Ω and *C*=500 µF
Ripple filter at PCC: R_f=5 Ω and C_f=5µF
DSTATCOM:
DC bus capacitor C_{dc} =3000 µF
DC bus Voltage: 400V
DC bus voltage PI controller: K_{dp}=0.5, K_{di}=0.8
AC bus voltage PI controller: K_{qp}=1.02, K_{qi}=0.65
PWM switching frequency: 20 kHz.

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